REMARKS

The Office Action of February 5, 2007 has been carefully reviewed.

Claim Objections

Claim 1:

As recommended by the Examiner, the preamble in all claims has been changed from "a processor unit" to -- a processor unit system -- removing the ambiguity possibly caused by later recitation to a component "processor unit".

The Examiner has recommended that the term "the processor units" in the limitation (ii) should be -- a plurality of processor units --. Applicant believes that the phrase "the processor units" refers to only two processor units: the "processor unit" at line 3 and the "another processor unit" at line 9 of the claim. Because many important applications of the invention will involve only two processor units: one executing the critical section and one creating a conflict, it is believed that reciting "a plurality of processor units" would unduly limit the invention to multiple conflict situations.

Claim 2:

The Examiner has recommended a similar change in claim 2, which is respectfully declined for the reasons described immediately above.

The change proposed by the Examiner in claim 2, limitation (c) has been made.

Claim 3:

Claim 3 has been amended to correct a typographical error with respect to a reference to an element of previous claim 2.

Claim 7 and 10:

The change proposed in claim 7, of changing "the processor" to --the processor unit-- has been made, however, this change appears to already have been implemented in claim 10. As noted by the Examiner, claim 10 should depend upon claim 2 and this change has been made.

Claim 14:

The change proposed by the Examiner to claim 14 has been implemented.

Claim Rejections -- 35 U.S.C. §112

Claims 4 and 5:

Claims 4 and 5 have been rejected as unsupported by the specification and/or for ambiguity. These claims are intended to describe the fact that standard cache coherence protocols, for example, may be used to handle conflicting demands for given data, by the different processing units, absent the execution of a critical section. Claim 4 has been amended to express this concept more simply.

Support for claims 4 and 5 is found, for example, at paragraphs [0043] and [0044] of the published application, which describe the use of standard memory protocols such as cache coherent protocols. The fact that these protocols are relied upon, absent treatment of conflicts in critical sections, is described in the published application at paragraphs [0017] and [0018] as well as elsewhere in the application. Applicant is uncertain as to the precise point of the confusion but is open to other claim amendments that may correct this problem.

Claim 9:

Claim 9 has been objected to with respect to the phrase "a counter sets itself to the timestamp of the request of the second processor unit" in view of the fact that the counter is described as a "globally unique clock". Applicant believes the confusion here arises from the fact that the phrase "globally unique clock" sounds like there is only one clock rather than multiple clocks each having a unique clock value. Accordingly, Applicant has amended the claims to change "globally unique clock" to be --clock with a globally unique value--.

Generally, each clock has a counter section counting occurrences of critical sections that provides a time-like value and also a second portion holding a number that is unique for each processing unit to ensure that no two clocks have the same clock value such as would create a tie when attempting to resolve an ordering for acquisition of critical data.

Claims 2, 21, and 22:

Claims 2, 21 and 22 have been rejected based on ambiguity in the claim language. The Applicant has adopted the approach proposed by the Examiner of using a conditional formulation beginning with "if the second processor unit..."

Claim 10:

The antecedent basis problems of claim 10, as noted by the Examiner, have been corrected.

Claim 15:

The objected phrase in claim 15 has been corrected to now read "respond to a probe message from a second processor unit".

Claim Rejections-35 U.S.C. §103

The rejection of claims 1, 10, 11, 16, 17-20, and 23 under 35 U.S.C. §103(a) as being unpatentable over Srinivas in view of Applicant's admitted prior art.

As noted by the Examiner, Srinivas teaches a system of allowing multiple processors to access shared data without the use of locks. The shared data in this case are singly linked lists which can have data added to or removed from the front or back of the list. Srinivas accomplishes this task through the use of an atomic instruction "compare and swap" that cannot be interrupted by other contending processing units. See generally, Srinivas at column 3, lines 15 through 19.

In this respect, Srinivas is analogous to the prior art acquisition of the lock itself described at paragraph [0005] of the published present application. Technically, this acquisition of the lock variable is done without the use of locks (otherwise there would be no end to the number of lock variables needed--each lock requiring a lock in turn to ensure that it is accessed only by one processing unit).

The technique of Srinivas and the technique of initially acquiring a contested lock variable as described in the background of the present application, works only because the modification of the contested data is extremely simple. For this reason, a person of ordinary skill in the art would know that the Srinivas approach would not work in cases where the processing unit needed to retain the contested data for a number of instruction cycles -- for example, as would be the case for data on seat reservations in an airline ticketing system.

Based on this understanding, Srinivas fails to teach a number of the elements of claim 1 of the present invention. First, there is no "conflict resolution circuit" as claimed because there

is no conflict possible in Srinivas. The use of an atomic instruction eliminates conflict because the instruction is complete before any other instructions can interrupt it.

Second, there is no evidence that Srinivas "detects a critical section" in the executing program. In fact, there would be not reason to detect the critical section in Srinivas because no conflicts are possible. The cited section of Srinivas of column 2, line 66 to column 3, lines 1, describes the elimination of locks but not the detection of a critical section. Srinivas is and can be oblivious to the existence of a critical section because no locks are used in Srinivas. Further, because Srinivas eliminates locks, it would appear to be difficult or impossible to determine whether a critical section had been entered.

Third, Srinivas fails to teach "establishing a priority between the processor units to resolve the conflict" without the acquisition of the lock as claimed. Because Srinivas avoids conflicts by using atomic instructions, no priority needs to be established. While a default priority does occur, it is not established by any mechanism of Srinivas but rather randomly. The protocol of LIFO or FIFO referred to in Srinivas concerns the limited operations that may be performed on the list data and is not a protocol for organizing the execution ordering of the processing units.

For these reasons, even assuming the missing element of speculative execution is provided by the Applicant's admitted art, the combination of the Applicant's admitted art and Srinivas fail to teach critical elements of the claim 1.

Applicant further believes that a person of ordinary skill reading Srinivas would not be led to combine Srinivas with the Applicant's admitted art. This is because Srinivas presupposes the ability to resolve the lock conflict problems with atomic instructions, something that would be evidently impossible in the context of the present invention. A person of ordinary skill in the art, understanding the ability to speculate in the execution of instructions, would still not necessarily be led to the present invention's solution of prioritizing the remaining processors to avoid the "live lock" problem. The motivation of saving wasted time would not lead one to prioritize the execution of the deferred processing units because the speculation itself is what saves time. Absent a recognition of the "live lock" problem described in paragraph [0056] of the present application, and an understanding of how prioritization can avoid a live lock

problem, the desire to save time by eliminating lock and unlock routines would be no motivation or guidance to the solution of the present invention.

The rejection of claims 21-22 over the above art in further view of Massalin is respectfully traversed. Applicant agrees that Massalin would have a processing unit with a clock but finds no evidence in Massalin that the clock would produce a "globally unique clock value" per the current amendment to claim 21, except by chance. Further, as noted above, Massalin doesn't teach or describe a "conflict resolution circuit". Further Applicant can find no evidence in Massalin that there is a comparison of timestamps, or any motivation to do such a comparison, to resolve conflicts. Massalin like Srinivas describes a system that uses atomic instructions to eliminate the need for locks and thus to eliminate conflicts.

The cited section of page 8 appears to describe a thread queue being a method of scheduling tasks in a multi-task operating system. Applicant cannot find any evidence that there is time stamping of the threads much less timestamping of requests for data subject to contention.

The rejection of claim 23 over Srinivas is respectfully traversed. As noted above with respect to claim 1, it is believed that Srinivas does not teach a "conflict resolution circuit" or a system that "detects a critical section". Further, for the reasons described above, it is believed that the Massalin reference would not be combined with the Applicant's admitted prior art absent some additional teaching suggestion not present in the cited art.

In light of the amendments and comments provided above, it is believed that claims 1 through 23 are now in condition for allowance, and allowance is respectfully requested.

Although no additional fees are believed due for filing this amendment, if an additional fee is deemed to be due, please charge any fee to Deposit Account No. 50-1170.

Respectfully submitted,

By: _____

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